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THERMAL CROSSTALK MODELLING OF THIN FILM RESISTOR ARRAYS

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Abstract

This paper describes the thermal modelling results for a thin film resistor array which can have applications in infrared scene projection. In this design, the array consists of two parallel rows of resistor elements. A central aluminium busbar which forms a common electrical connection for all resistor elements, also provides thermal isolation between the two rows through thermal connection to the array substrate. It is shown that the thickness of the aluminium busbar of the order of 2 μm is sufficient to provide good thermal isolation, thus allowing an increase in the pixel fill factor.

Keywords: infrared scene projector, thermal modelling, thin film resistor arrays

Introduction

Thin film resistor arrays are a promising candidate for use in infrared projector technology [1–5]. A pixel may be generated by a single resistor element, which is electrically heated such that grey body radiation in the infrared region is emitted. In the bilinear (two rows x n columns) array under study here, a single resistor element consists of a thin film resistor of nichrome measuring 320 μm×320 μm, and the whole array is fabricated on mesas of fully cured polyimide film deposited on a silicon wafer. Polyimide is used as the insulating layer as its thermal conductivity is of the order of 10^{-3} of silicon's. The polyimide thus provides the necessary thermal and electrical isolation from the silicon substrate. Silicon is chosen as the substrate material due to its well characterized thermal and electrical properties. By using silicon substrates, the incorporation of some type of on-chip electronic driving circuitry remains a useful option.

One of the factors that limits the pixel fill factor is the problem related to thermal crosstalk between pixels (resistor elements). Thermal isolation between adjacent elements within a single row and opposite elements in adjacent rows can be achieved by trenching the polyimide between elements. For example, in previous fabricated structures, isolation between elements within a row was done by separat-

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ing resistors with a 10 μm wide trench etched into the polyimide. An analysis of the effect of this trenching has already been performed [4]. However these versions of the bilinear array lacked a polyimide trench between the rows and the arrays exhibited unacceptable thermal crosstalk between the adjacent rows. These arrays used a common busbar structure and the aluminium busbar provided an excellent thermal path between opposing elements in the two rows. The thermal crosstalk from this structure was thus excessive. Consequently, a modified array structure was designed; this incorporates polyimide trenches between the rows and columns creating an isolated polyimide mesa for each resistor element. The aluminium busbar between the rows is retained, but as shown in Figs 1a and 1b, a major part of the width of the busbar is now in contact with the silicon substrate. As the thermal conductivity of silicon (1.5 W cm^{-1} °C^{-1}) is significantly higher than polyimide, the silicon now acts as a heat sink for the unwanted heat flux passing between the two rows. For the purpose of comparison, the original design without the trench is shown in Fig. 1c. It should be noted that the dimensions of the two designs are not the same.

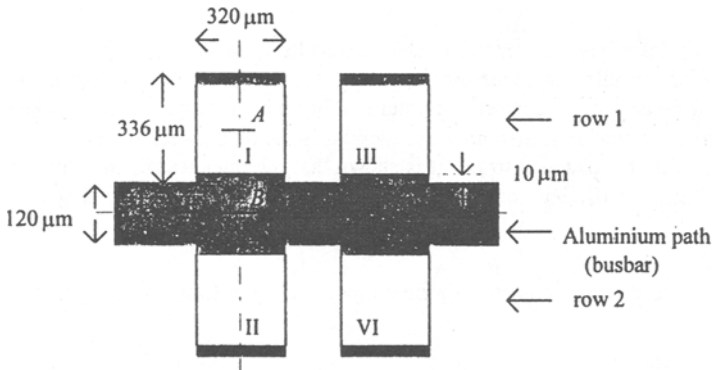

Fig. 1a Plan view (not to scale) of a partial resistor array on polyimide surface

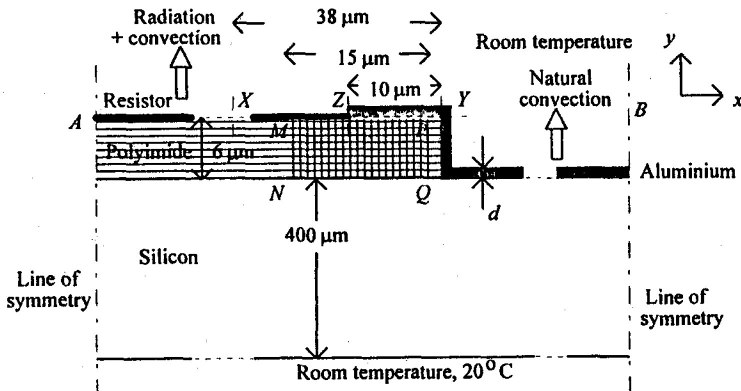

Fig. 1b Cross-section across *A–B* (not to scale) of Fig. 1a

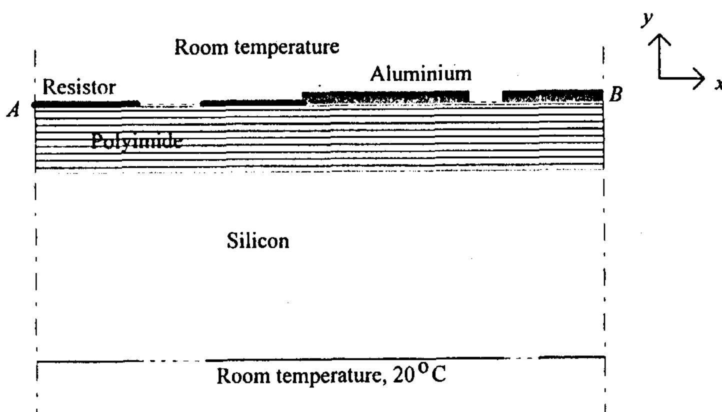

Fig. 1c Cross-section across A–B of the original design

In this paper, some thermal modelling results for crosstalk between rows in a bilinear array are reported. It is shown that with a suitable thermal conducting path (the aluminium busbar), the thermal crosstalk between the two rows is significantly reduced. A combination of the multigrid and the combined fine-coarse mesh techniques applied to the method of transmission-line modelling (TLM) [6] has been used to model this thermal problem. The temperature distribution along the length of a resistor element as well as the transient response has been calculated.

The model and method of solution

Figure 1a shows a plan view of four resistor elements of the resistor array, while Fig. 1b shows a cross-section taken from A–B of Figure 1a. It can be clearly seen from Fig. 1a that the aluminium busbar between the two resistor rows provides a thermal path between elements of the two rows. An analysis of the thermal crosstalk between elements I and III has been reported elsewhere [4, 5] and thus we shall concentrate on the crosstalk between elements I and II. The relevant dimensions and materials are given in Fig. 1b. The thermal field may be approximated by the well known diffusion equation in two dimensions:

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + Q = \frac{c\rho}{k}\frac{\partial T}{\partial t} \tag{1}$$

where c, ρ, k and T are the specific heat, density, thermal conductivity and temperature respectively. Typical values for the materials used in the fabrication of the array may be found in [4]. Q is the heat source and is zero except within the heated element.

The entire field region is discretised and solved by the method of transmission-line modelling (TLM) using a combination of the multigrid and the improved combined fine-coarse mesh techniques described in [6]. The method of TLM is an ex-

plicit time-stepping algorithm originally developed by Johns [7]. The use of the multigrid technique and the combined fine-coarse mesh technique can be found in [8] and [9] respectively. Implementation detail of this method is not discussed here. The minimum mesh size used (the heated region and around the surface) in this study is 2/9 μm and the maximum is 6 μm (within the silicon and part of the polyimide). Each resistor element is assumed to be dissipating 1 W(≈9.19 MW m^{-2}). Due to the small thickness (typically 12 nm) of the resistor, heat is assumed to be generated at the surface. Other boundary conditions are shown in Fig. 1b. The aluminium thickness, d was varied from 0 to 2.0 μm and the two dimensional temperature distribution patterns were determined iteratively until a steady state was achieved.

Results

Typical isotherm plots with and without (d=0) the aluminium busbar are shown in Figs 2a and 2b respectively. The case of d=0 shows the effect of removing any heat transfer via the busbar to the silicon substrate, while in Fig. 2b the introduction of a heat path effectively confines the generated heat to the Z–M (lefthand) portion of the resistor. The penalty for introducing this isolation is a small reduction in the resistor temperature at each end of the resistor. However, this effect disappears on moving towards the centre of the resistor as shown in Fig. 3 where the surface tem-

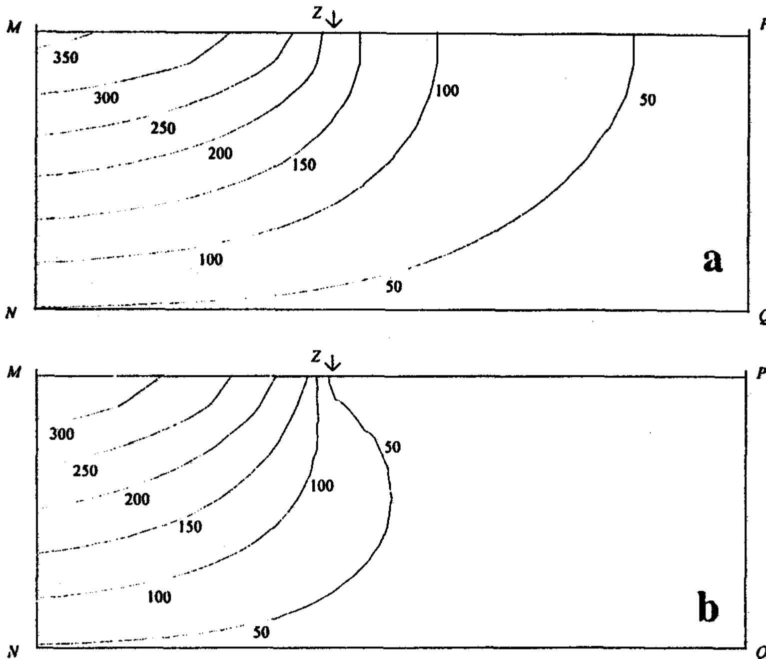

Fig. 2 Isotherms of the shaded section $MNPQ$ (MN=6 μm and MP=15 μm) of Fig. 1b; temperatures in °C. a) d=0; b) d=2 μm

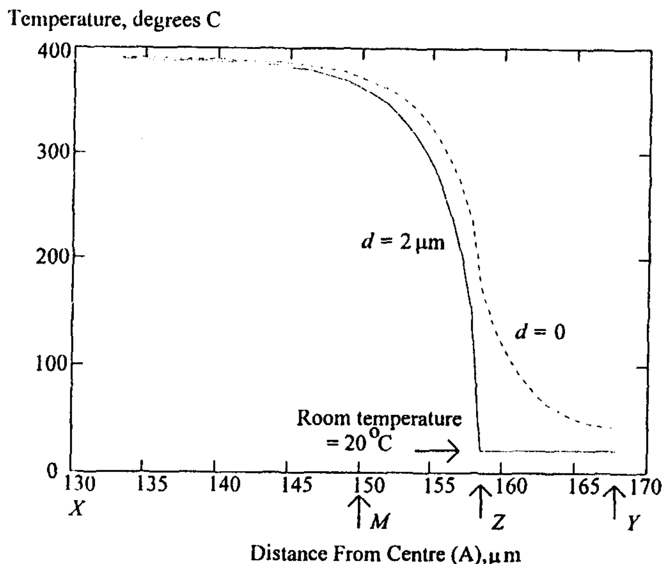

Fig. 3 Steady state surface temperature distribution along the line X–Y of Fig. 1b for d=0 and d=2 μm

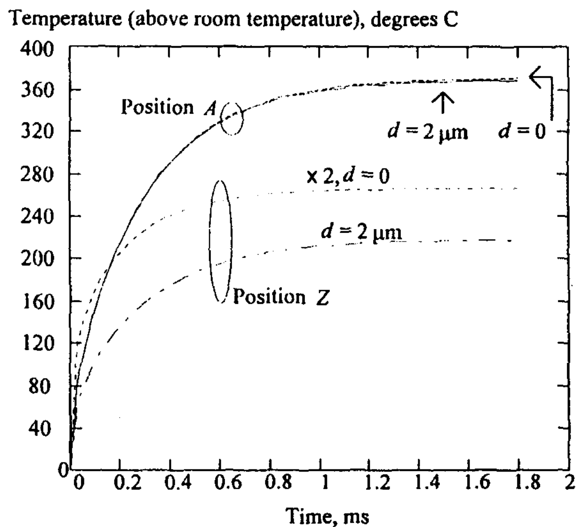

Fig. 4 Step responses of the heated resistor element at positions A (centre of resistor) and Z (interface between resistor and polyimide/aluminium)

perature distributions along the line X–Y of Fig. 1b are plotted. Figure 4 shows the transient response of the temperature of a resistor element at points A and Z (Fig. 1b) due to a step heat source input. The 10–90% rise time is of the order of

600 μs at point A and reduces to around 400 μs at the resistor-aluminium junction (point Z). The value at point A is somewhat shorter than the 1000 μs reported for a similar structure in [5] – however in [5] the polyimide thickness is 10 μm and the increased thermal mass associated with 10 μm would account for the longer rise time. From Fig. 4, the influence of the busbar on rise times is only apparent at the ends of the resistor with rise times away from the ends being little affected by the aluminium. It is clear that allowing the aluminium busbar to come into contact with the silicon substrate provides a very effective way of reducing the unwanted thermal crosstalk between elements. Although a thinner aluminium busbar than 2.0 μm may be used to achieve thermal isolation, a thickness of 2 μm has been found desirable in order to achieve reliable busbar to resistor interconnects. With the improved thermal isolation a reduction in the separation between rows could be contemplated, thus improving the fill factor.

Conclusion

Modelling results show that by using a central aluminium busbar in contact with the substrate, the thermal crosstalk problem between rows of resistor elements in a bilinear array may be considerably reduced. In order to achieve adequate thermal isolation and to satisfy practical fabrication requirements, an aluminium thickness of around 2 μm is considered appropriate.

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